

# icAS/Ip

## (Async to Sync Interface Converter)

### DESCRIPTION

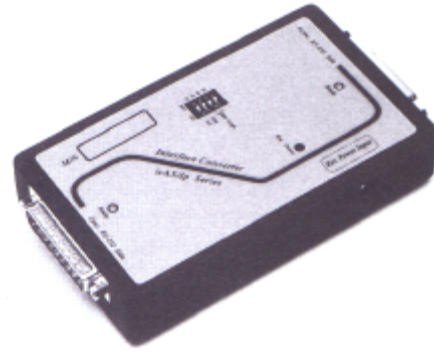
- ◆ The **icAS/Ip** interface converter allows full conversion between a computer/terminal asynchronous port and a synchronous modem.
- ◆ The **icAS/Ip** conforms to the CCITT V.22 standard of conversion and accommodates the difference in frequency between the async port and sync modem.
- ◆ The **icAS/Ip** derives its baud rate automatically from the transmit clock of the modem and operates at data rates from 300 to 19200bps
- ◆ The functions below can be selected by DIP-switch from the front panel:

Character Length :8,9,10,11 bits  
 Start/stop bit :1 start and 1 stop  
 Parity bit :with or without

- ◆ The **icAS/Ip** is completely transparent to data/protocol, with no limitation for block size.
- ◆ To prevent transmission errors the unit provides:  
 4 bit buffer, transmit side  
 15-18bit buffer, receive side
- ◆ When the transmitted async data frequency exceeds the sync, up to one in every four stop bits may be removed. Conversely, if the frequency is less than sync, stop bits will be added.
- ◆ The **icAS/Ip** recognizes start and stop bits at the receiving end. If a missing stop bit is detected, then the stop bits are shortened during each character transmission by a percentage. The percentage is strap selectable for either 12.5 or 25%.
- ◆ The **icAS/Ip** is transparent to any length of break signals.
- ◆ The “RTS extend” and “DCD extend” enable operation in multi-point applications. The implementation is as follows:
  - ◇ The RTS (sync side) is raised immediately when RTS is raised on the async side.
  - ◇ When RTS drops on the async side, the RTS drop on the sync side is delayed by a four bit interval.
  - ◇ The DCD (async side) is raised immediately when DCD is raised on the sync side.
  - ◇ When DCD drops on the sync side, the DCD drop on the async side is delayed by a 24 bit interval.

### FEATURES

- ◆ Enable async terminals to use sync modems and meet CCITT V.22 standard.
- ◆ Does not require AC power adapter, powered directly from the interface lines.
- ◆ Automatic baud rate adjustment from 300 to 19.2kbps.
- ◆ Fully transparent.



### SPECIFICATIONS

- ◆ Transmission format  
 async to sync conversion  
 transparent to protocol
- ◆ Data rate  
 automatic, 300 to 19.2kbps
- ◆ Number of data bits  
 selectable 8,9,10,11, 1 start and 1 stop, with or without parity
- ◆ Buffer  
 transmit :4 bits  
 receive :15 to 18 bits (depending upon the selected character length)
- ◆ Frequency allowance selectable  
 12.5% allows frequency difference between async and sync of -2.5 to +1.0%  
 25% allows frequency difference between async and sync of -2.5 to +2.5%
- ◆ Interface  
 EIA RS232C / CCITT V.24
- ◆ Connectors  
 sync side :DB25M built in unit  
 async side :DB25F built in unit
- ◆ DIP switch  
 Select data length (positions 1 and 2, refer to table 1) and ESR (Extended Signaling Rate, position 3, table 2). The switch selection is clearly marked on the front panel of the converter.
- ◆ Power Source  
 No AC power is required. Unit used ultra-low power derived from the data and control signals on both the sync and async sides.  
 sync side :3,5,6,8,9,15,17  
 async side :2,4,9,20
- ◆ Environment  
 Temperature :0-50°C / 32-122°F  
 Humidity :up to 95% non-condensing
- ◆ Dimensions :73mm(L) \* 53mm(W) \* 20mm(H)
- ◆ Weight :145g net

**Table 1- Async character bit length setting**

start bit	data bits	parity bits	stop bits	number of bits	SW. S1	SW. S2
1	5	none	2	8	OFF	ON
1	5	odd, even	1,1.5	8	OFF	ON
1	6	none	1	8	OFF	ON
1	5	odd, even	2	9	ON	ON
1	6	none	2	9	ON	ON
1	6	odd, even	1,1.5	9	ON	ON
1	7	none	1	9	ON	ON
1	6	odd, even	2	10	OFF	OFF
1	7	none	2	10	OFF	OFF
1	7	odd, even	1,1.5	10	OFF	OFF
1	8	none	1	10	OFF	OFF
1	7	odd, even	2	11	ON	OFF
1	8	none	2	11	ON	OFF
1	8	odd, even	1,1.5	11	ON	OFF

**Table 2- ESR settings (Extended Signaling Rate)**

SW - S3	Extended Signaling Rate
OFF	-2.5% to +1.0%
ON	-2.5% to +2.5%

## APPENDIX

**PRODUCT** : icAS/Ip (ASYN to SYNC interface converter)  
**Subject** : PCB/Cable pin assignment

**Table 1 : Asynchronous side pin assignment**

ASYN side DB25/PCB		ASYN side DB25/Cable		Description	Direction
Pin No.	Circuit	Pin No.	Circuit		
1	FG	1	FG	Protective Ground	
2	TD	2	TD	Transmitted Data	from DTE
3	RD	3	RD	Received Data	to DTE
4	RTS	4	RTS	Request to Send	from DTE
5	CTS	5	CTS	Clear to Send	to DTE
6	DSR	6	DSR	Data Set Ready	to DTE
7	GND	7	GND	Signal Ground	
8	DCD	8	DCD	Data Carrier Detect	to DTE
9	+9V/IN	9	+9V/IN	External DC 9V Power IN	from DTE
20	DTR	20	DTR	Data Terminal Ready	from DTE

**TABLE 2 : Synchronous side pin assignment**

SYNC side DB25/PCB		SYNC side DB25/Cable		Description	Direction
Pin No.	Circuit	Pin No.	Circuit		
1	FG	1	FG	Protective Ground	
2	TD	2	TD	Transmitted Data	from modem
3	RD	3	RD	Received Data	to modem
4	RTS	4	RTS	Request to Send	from modem
5	CTS	5	CTS	Clear to Send	to modem
6	DSR	6	DSR	Data Set Ready	to modem
7	GND	7	GND	Signal Ground	
8	DCD	8	DCD	Data Carrier Detect	to modem
9	+9V/IN	9	+9V/IN	External DC 9V Power IN	from modem
15	TC	15	TC	Tx Signal Element Timing(DCE)	from modem
17	RC	17	RC	Rx Signal Element Timing(DCE)	from modem
20	DTR	20	DTR	Data Terminal Ready	to modem
24	XTC	24	XTC	Tx Signal Element Timing(DTE)	to modem